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APPLICATION FOR PATENT

ON

A HIGHLY EFFICIENT, HIGH CURRENT DRIVE, MULTI-PHASE VOLTAGE MULTIPLIER

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A HIGHLY EFFICIENT, HIGH CURRENT DRIVE, MULTI-PHASE VOLTAGE MULTIPLIER

FIELD OF THE INVENTION

[0001] The present invention generally relates to the field of integrated circuits, and particularly to a voltage doubling and voltage regulating integrated circuit.

BACKGROUND OF THE INVENTION

[0002] Voltage multipliers are used in various applications where a device or circuit, such as an integrated circuit, requires a higher voltage than that provided by the power supply. The voltage multiplier can only supply up to a certain rated current that is less than the power supply maximum current. During each clock cycle, enough charge must be moved from the doubling capacitors to the load capacitors to support the maximum rated current for an entire clock cycle until the next pulse of charge is delivered to the load. To increase the amount of load current the multiplier can supply, the designer generally can either add capacitance or increase the clock frequency (thereby increasing the number of times per second the charge is deposited on the load). There are two problems associated with adding more capacitance in conventional voltage multiplier circuits. One problem is that the buffers needed to drive these capacitors become very large. As the charging capacitors increase in size, the power needed to supply them with 'fast' edges increases exponentially. The reason for this is the non-ideality of the inverters and their increasing ON resistance as the voltage at their outputs nears VDD or VSS. Therefore, increasing the capacitor size to increase output drive will begin to lower the multiplier's efficiency and, at some point, the inefficiency of the multiplier will limit the design. The second problem introduced by increasing capacitor size is that the switches needed to carry the charge to the output capacitor become very large since they must be in or near their triode region during normal operation. Increasing the frequency of the clock increases the current driving capabilities of the voltage multiplier to a certain point. Then, the efficiency of the multiplier begins to go down dramatically. One reason

for this is that the clocks entering the multiplier must never be at a LOW level at the same time (i.e., the inactive or LOW level portions must be non-overlapping). This requirement means that at higher frequency operation, the active level overlap time becomes a much larger percentage of the clock period. Another reason the multiplier becomes less efficient as the frequency increases is that the ability for charge to actually transfer from the multiplying capacitors to the load capacitor diminishes as the time of transfer goes down. These fundamental problems limit voltage multipliers to low current applications and limit their overall usefulness.

[0003] Therefore, it would be desirable to provide a highly efficient high current voltage multiplier.

SUMMARY OF THE INVENTION

[0004] Accordingly, the present invention is directed to a circuit and method for supplying voltage multiplication at an 'effective' high frequency of operation and with large current drive capabilities.

[0005] In a first aspect of the present invention, a high current, multi-phase voltage multiplier includes a multiple phase active level overlapping clock generator that generates a plurality of unique phase clocks. Each phase clock is paired with another phase clock such that the two phase clocks of a pair are never inactive at the same time. The phase clock pairs each activate a charging circuit that includes two pairs of voltage dividers and two charging capacitors. The voltage dividers are each formed of two switches (or other active or passive elements) tied together. Preferably, the two switches are an NMOS transistor and a PMOS transistor electrically connected through their respective drain terminals. The charging capacitors are driven by the multiple phase active level overlapping clock generator.

[0006] In a second aspect of the present invention, a method for multiplying a voltage involves setting a length of the phase clock period and setting a duty cycle that favors the active HIGH level. The phase clocks are paired such that at least one of the phase clocks is at the HIGH level. The phase clocks are used to charge and discharge capacitors that drive the voltage multiplication circuitry.

[0007] The circuit of the present invention solves the problems associated with high load current voltage multiplier circuits. The circuit reduces the inefficiency due to the active level overlapping portion of the clock at high frequencies. It reduces the inefficiency due to extremely large drive currents on the inverters supplying current to the multiplying capacitors C1(*) and C2(*). It increases the efficiency of the multiplier by allowing M-1 phases to charge the output at any given time and also increases the time given to each capacitor to fully charge and discharge. The multi-phase voltage multiplier has an added benefit that the ripple on the output is much smaller than in single phase multipliers. This multi-phase voltage multiplier is unique in that it can supply very large current to the load and remain very efficient.

[0008] It is to be understood that both the forgoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention as claimed. The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention and together with the general description, serve to explain the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0009] The numerous advantages of the present invention may be better understood by those skilled in the art by reference to the accompanying figures in which:

FIG. 1 illustrates a preferred embodiment of the circuit of the present invention;

FIG. 2 illustrates an alternative embodiment of the circuit using diodes instead of PMOS transistors;

FIG. 3 illustrates an embodiment of a method of the present invention; and

FIG. 4 illustrates waveforms provided by the circuit of FIG. 1.

DETAILED DESCRIPTION OF THE INVENTION

[0010] Reference will now be made in detail to the presently preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

[0011] The present invention relates to a circuit and method for a high current, high frequency voltage multiplier. In the present invention, parallel circuit combinations perform a twice per phase clock charge pump and dump onto the voltage multiplier output line. Multiple parallel circuit combinations, each slightly out of phase with the others, ensure that the multiplier output continually has available a sufficient amount of charge for a driving current. Each parallel circuit combination includes two voltage dividers and two charging capacitors. The voltage dividers are formed from active or passive elements tied together: one end is fed through the power supply, the middle controls charging and discharging, and the other end provides the multiplied voltage.

[0012] The voltage multiplier of the present invention uses multiple clock phases to relieve the problems associated with conventional voltage multipliers. By using multiple, slower clock phases to provide charge to the output, several benefits are realized: the size of each multiplying capacitor is reduced, the time each multiplying capacitor has to discharge onto the load capacitor remains large, and the active level overlap time of the clocks becomes a lower percentage of the clock period. The buffers used to drive the multiplying capacitors can be reduced and the current needed to supply 'fast' edges to these clocks is reduced significantly. An added benefit of the present invention is that the amount of voltage ripple on the load decreases significantly from a design that uses larger capacitors or a higher frequency to create a higher drive current. Since only a portion of the charge is delivered to the load each phase during a much lengthened delivery (or, charge transfer) time, ripple is very small on the load. If there are M clock phases, at any

given time, at least M-1 charging capacitors are supplying charge at the same time. The active level overlap time becomes a much smaller percentage of the overall period. Since the multiplier is not delivering charge when the clocks are both at a HIGH level, active level overlap time results in inefficiency. By using multiple clock phases, the percentage of time the clocks are overlapped at the active HIGH level is reduced as described by the relationship Tnol(mf)=Tnol(ck)/M, where M is the number of clock phases, Tnol(mf) is the percentage of time the dual phase clocks are active level overlapped in multiple dual phase clocks, and Tnol(ck) is the percentage of time the clocks are active level overlapped in a single dual phase clock pair. For example, if the efficiency due to active level overlapping clocks for the single dual phase clock is approximately 66%, meaning the single dual phase clocks are active level (i.e., HIGH level) overlapping 1/3 of the time, then by using two dual phase clock pairs, the efficiency due to active level overlapping clocks is now approximately 83% (clocks active level overlap 1/6 of the time) and, for four dual phase clock pairs, the efficiency would not be approximately 92% (clocks active level overlap 1/12 of the time). This shows the enormous advantage of using multiple dual phase clock pairs instead of a single dual phase clock pair.

[0013] FIG. 1 illustrates a preferred embodiment of the circuit of the present invention. An M phase clock generator provides 2*M clocks or M pairs of active level overlapping phase clocks. The term "active level overlapping" refers to the simultaneous occurrence of the active HIGH portion of the two phase clocks of a dual phase clock pair. If the two phase clocks of a pair were to overlap their inactive low portions, power would be drained from the doubled voltage output VHH. In FIG. 1, each phase clock Ph1(*), Ph2(*) is buffered by a buffer Buffer1 (*), Buffer2 (*). The buffer may be an inverter, a pair of inverters, or other circuitry that isolates the clock generator from the voltage multiplier circuitry. Each buffer drives a charging capacitor C1(*), C2(*). Switches are controlled through nodes v1 and v2. Preferably, the switches are field effect transistors. Bipolar transistors may be used in alternative embodiments. More preferably, the switches in a voltage divider are a P type MOSFET (i.e., PMOS transistor) to provide the

multiplied voltage output and an N type MOSFET (i.e., NMOS transistor) through which current from voltage source VDDA is used to charge the capacitor C1(*), C2(*). The transistors and corresponding charging capacitor form an RC circuit whose time constant limits the phase clock frequency. For example, if the transistors are 100 ohms each and the capacitor is 10 picofarad, then the RC time constant (i.e., time to reach 63% of the final value) is about 1 nanosecond. The output signal from the PMOS transistors MP1(*), MP2(*) are tied together. To provide protection to the voltage multiplier circuitry, a protective diode (i.e., a P-N junction) may be added to each pair of coupled voltage dividers so as to permit charge flow in one direction only (i.e., the output). In an alternative embodiment, the PMOS transistors may be replaced with diodes.

[0014] The circuit of FIG. 1 alleviates the problems associated with high current draw voltage multipliers. Each phase of the voltage multiplier (multiplication M = 2 in this version) operates as follows and is equivalent to a conventional single clock voltage multiplier. As phase clock PH1(*) rises to a HIGH level, the voltage at V1(*) rises from VDDA to approximately 2*VDDA. At this point, both transfer switches MP1(*) and MP2(*) are both off. Thus, there is no charge flowing to the output when the phase clocks PH1(*) and PH2(*) are both at a HIGH level (i.e., active level overlap time). Later, when PH2(*) falls to a LOW level, MN2(*) is turned ON and V2(*) discharges through MN2(*) which is controlled by V1(*). The charging capacitor C1(*) discharges some of its charge through MP1(*) onto output capacitor CLOAD during the time when V2(*) is at VDDA and MP1(*) is on. The speed at which the charge flows from C1(*) onto output capacitor CLOAD is inversely proportional to the size of CLOAD and the ON resistance of transfer switch MP1(*). In other words, the speed of charge flow is related to the RC time constant product of the ON resistance of the transfer switch and the capacitance of the output capacitor CLOAD. In the case where the ON resistance is 100 ohms and the capacitance of the output capacitor is 10 picofarads, the charge flow is 63% completed after one nanosecond and 86% completed after two nanoseconds. The phase clock PH2(*) then becomes a HIGH level and V2(*) rises to a HIGH level of

approximately 2*VDDA. At this point, both transfer switches MP1(*) and MP2(*) are both off again and there is no charge flowing to the output and phase clocks PH1(*) and PH2(*) are both HIGH (active level overlap time). When the phase clock PH1(*) falls to a LOW level, MN1(*) is turned ON, and V1(*) discharges through MN1(*) which is controlled by V2(*). The charging capacitor C2(*) discharges some of its charge through MP2(*) onto output capacitor CLOAD during the time when V1(*) is at VDDA and MP2(*) is on. At this point, the process repeats. In order to supply enough current to the load during each clock cycle, the multiplier must transfer Q = I/T charge onto output capacitor CLOAD to sustain the voltage level VHH (I is the load current, T is the input clock period). The output capacitor CLOAD acts as a smoothing capacitor and a glitch filter. The multiplied voltage output may be further filtered; for example, by adding an inductor in the output path. Other output filter combinations may be used.

[0015] The operation of the multi-phase clocked voltage multiplier is described by referring to Figure 1 again. As the phase clock PH1(1) rises to a HIGH level, the voltage at V1(1) rises from VDDA to approximately 2*VDDA. When the phase clock PH2(1) falls to a LOW level, MN2(1) is turned ON, and V2(1) discharges through MN2(1) which is controlled by V1(1). The charging capacitor C1(1) discharges some of its charge through transfer switch MP1(1) onto output capacitor CLOAD in the portion of time when V2(1) is at VDDA (a LOW level relative to VHH) and MP1(1) is on. The phase clock PH2(1) remains at a LOW level, allowing charge to continue to flow from C1(1) to CLOAD. The phase clock PH1(2) rises to a HIGH level. Thereafter, when the phase clock PH2(2) falls to a LOW level, MN2(2) is turned ON, and V2(2) discharges through MN2(2) which is controlled by V1(2). The charging capacitor C1(2) discharges some of its charge through MP1(2) onto output capacitor CLOAD during the time when V2(2) is at VDDA and MP1(2) is turned ON. The same operational steps are performed for all the phases. Thus, phase clock PH1(3) rises to a HIGH level, then phase clock PH2(3) falls to a LOW level, phase clock PH1(4) rises to a HIGH level, then phase clock PH2(4) falls to a LOW level, and so forth, until PH1(M) becomes HIGH, then phase clock PH2(M) falls

to a LOW level. At any given time, either M or M-1 phases are simultaneously delivering charge to output capacitor CLOAD. The phase clock PH2(1) rises to a HIGH level and V2(1) rises to a HIGH level of approximately 2*VDDA. Although there is no charge being delivered from this phase of the multiplier, the output capacitor CLOAD is still receiving charge from phases 2 through M at this point. When the phase clock PH1(1) falls to a LOW level, MN1(1) is turned ON, and V1(1) discharges through MN1(1) which is controlled by V2(1). The charging capacitor C2(1) discharges some of its charge through MP2(1) onto the output capacitor CLOAD during the time when V1(1) is at VDDA and MP2(1) is on. Now each phase will continue this process; that is, PH2(2) rises to a HIGH level, then PH1(2) falls to a LOW level, PH2(3) rises to a HIGH level, then PH1(3) falls to a LOW level, and so forth, until PH2(M) rises to a HIGH level, then PH1(M) falls to a LOW level. At this point, the process repeats. It is obvious that there is no time when charge is not being delivered to the load by at least M-1 phases. This allows all the multiplying capacitors C1(*) and C2(*) to discharge and charge more completely.

[0016] FIG. 2 illustrates an embodiment in which the PMOS transistors have been replaced by diodes.

[0017] FIG. 3 illustrates an embodiment of a method of the present invention. The clock period of the basic phase clocks may be set through circuit design or be made adjustable through software inputs to a register 310. The basic phase clocks may be generated through software code. The duty cycle may be similarly set through hardware circuit design, through programmable registers, or through software code 320. A plurality of active level overlapping phase clock pairs are selected 330. If the selection is performed through software code, an operator may vary the number of phases to optimize performance. The selection may be hardwired through the circuit design. The method is used to charge and discharge capacitors associated with each phase clock pair 340.

[0018] FIG. 4 illustrates the timing waveforms of the plurality of active level overlapping phase clocks. A 5/8 or 62.5 % duty cycle is shown. Variations of the present invention allow for a different duty cycle such as 5/6, 2/3, 8/9, 9/16, and the like. In the present invention, each phase clock has a unique phase and all phase clocks are otherwise identical or essentially identical. The inactive portions of the two phase clocks in a pair never overlap.

[0019] Variations of the present invention may be implemented. For example, duty cycle processing may be accomplished through various Booleans expressions. Alternatively, flip flops may be used to provide the phase clocks. The supply voltage VDDA may be provided to the voltage multiplier through a current limiting resistor or through a capacitor. Varying the multiplication factor may be accomplished by various techniques. The multiplication factor may be a fraction, such as 2/3 or 1/2 , or may be a number greater than one, such as 1.5, 3, or 4. Instead of a voltage divider formed of one NMOS transistor and one PMOS transistor tied together at their drains, two PMOS transistors may be arranged with one NMOS transistor. The transistors may also be scaled dimensionally so as to vary their effective resistance. There are many ways to make voltage multipliers, such as though a capacitor and a diode or through various combinations of capacitors, diodes, resistors, and transistors. The multi-phase technique may be used for all clocked multipliers to increase current capabilities, efficiency, etc.

[0020] It is believed that the present invention and many of its attendant advantages will be understood by the forgoing description. It is also believed that it will be apparent that various changes may be made in the form, construction and arrangement of the components thereof without departing from the scope and spirit of the invention or without sacrificing all of its material advantages, the form hereinbefore described being merely an explanatory embodiment thereof. It is the intention of the following claims to encompass and include such changes.